A NEW FET FREQUENCY MULTIPLIER

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Abstract— **A new FET frequency multiplier is presented. The FET multiplier works in a similar way as a resistive mixer. The FET can be operated either as a series or as a parallel switch. The multiplier has essentially no DC power dissipation and its stability properties are good, since the drain-to-source bias-voltage is zero. The multiplier is insensitive to device parameter variations. Different configurations are analysed. The preliminary measurements show a conversion efficiency of -4.5 dB, which can be improved.**

I. Introduction

Frequency multipliers are often used in the local oscillator chain of micro and millimeter-wave communication systems. Today, FET-based frequency multipliers are widely used due to their relatively low cost and good conversion efficiency. For active FET multipliers, conversion gain has been demonstrated up to millimeter wave frequencies. Active multipliers are normally biased near pinch off with a relatively high drain-to-source bias voltage ($V_{ds,DC}$) [1,2,3]. In addition, they need high RF input power to achieve low sensitivity to device parameter variations. This way of operating the transistor has some less favourable characteristics such as poor stability properties and high DC power dissipation. It also requires accurate device models in order to optimise and predict the performance. The high RF input power might affect the lifetime of the transistor due to rectified current in the gate-channel junction.

We propose a new FET frequency multiplier topology [4,5]. The multiplier works analogues to a resistive mixer. However, since the multiplier has only one input signal, it mixes the input signal with itself to generate higher order harmonics. The multiplier has good stability properties, low sensitivity to device parameter variations and essentially no DC power dissipation, since the FET operates in the resistive region. The multiplier performance is also insensitive to the RF input power.

II. Principle of operation

The idea behind this frequency multiplier is to perform resistive mixing in the FET channel to generate harmonics of the input frequency. A schematic diagram of the multiplier is shown in Fig. 1. The input signal (at the frequency ω) is fed to both the gate and the drain of the FET, where the major part of the power is fed to the drain. The voltage at the gate controls the channel conductance. Therefore, the channel-current (i_{ds}) generated by v_{ds} will be amplitude modulated by the gate-to-source voltage (v_{gs}). The amplitude modulation gives rise to currents at DC, ω, 2ω, ..., $n\omega$. The desired harmonic is extracted with a filter at the drain. This filter is also used to terminate undesired frequencies, improving the conversion efficiency of the multiplier.

Besides filtering, the performance of the multiplier can also be optimised by changing the conductance wave from. There are mainly three parameters which affect the conductance wave form: the gate-to-source bias-voltage ($V_{gs,DC}$), the voltage swing at the gate (V_{gs}) and the phase offset, φ, between the drain and gate signal. The gate-bias and the gate voltage swing determine the duty-cycle and the conductance wave form. The phase offset, φ, determines during which interval, of the v_{ds} period, the FET will conduct. The phase offset can be used to reduce to DC-mixing term and, thus, to increase the conversion efficiency of the multiplier.

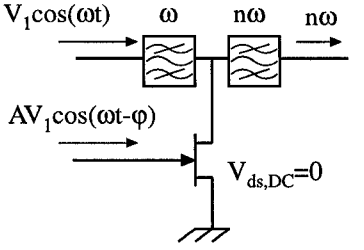

Fig. 1, A FET operated as a resistive multiplier

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III. Analysis

To analyse the multiplying properties of the FET we first approximate it with a time dependent conductance, and apply an input signal over the time dependent conductance. The input signal and the time dependent conductance have the same fundamental frequency, see Fig. 2.

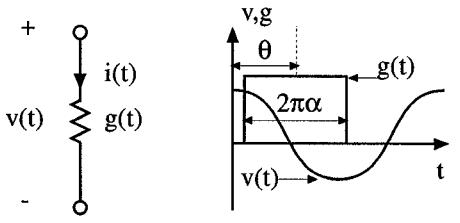

Fig. 2, Time dependent conductance and input signal.

We write the input signal voltage as

$$v(t) = A\cos(\omega t) \tag{1}$$

and the conductance wave form as

$$g(t) = \begin{cases} 0, & 0 \le \omega t < \theta - \pi\alpha \\ g_0, & \theta - \pi\alpha \le \omega t \le \theta + \pi\alpha \\ 0, & \theta + \pi\alpha < \omega t \le 2\pi \end{cases} \tag{2}$$

The current generated in the conductance can be expanded into a Fourier series and the frequency components are DC, ω, 2ω, 3ω, … . The multiplier performance can be optimised by changing the duty-cycle, α, of conductance wave form and by changing the phase, θ, between $v(t)$ and $g(t)$. The optimum α depends on the conductance wave form and the desired output harmonic, n, by assuming a rectangular conductance wave form it is[6],

$$\alpha = \frac{1}{n} \tag{3}$$

To achieve a zero DC-mixing component θ should be.

$$\theta = \frac{\pi}{2} rad = 90° \tag{4}$$

To implement a time dependent conductance we use a FET. The channel conductance of the FET is made time dependent by applying a signal to the gate. Two possible configurations are shown in Fig. 3.

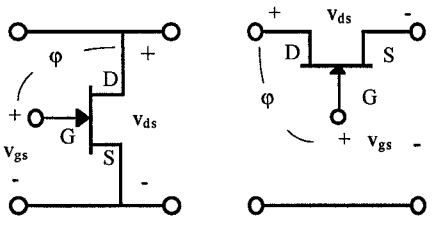

Fig. 3, FET as time dependent parallel/series conductance

For a FET, (4) implies that the trajectory described by the voltages v_{gd} and v_{gs} in the FET (Fig. 3), should be symmetrical with respect to v_{ds}=0 in the v_{gd}-v_{gs} plane (Fig. 4). To achieve this the phase offset between v_{ds} and v_{gs}, φ, should be

$$\varphi = Arc\cos(\frac{V_{ds}}{2V_{gs}}) \tag{5}$$

where

$$v_{ds}(t) = V_{ds} \cdot \cos(\omega t), \qquad V_{ds} > 0 \tag{6}$$

$$v_{gs}(t) = V_{gs,DC} + V_{gs} \cdot \cos(\omega t + \varphi), \quad V_{gs} > 0 \tag{7}$$

Fig. 4 shows a contour plot of the channel current versus v_{gd} and v_{gs} together with three different voltage trajectories corresponding to the values in table 1. From this we see that (B) will generate a DC-component. We also conclude that we need a large V_{gs} compared to V_{ds} to obtain a rectangular shape of the conductance wave form (A). This is because the more rectangular wave form the better conversion efficiency.

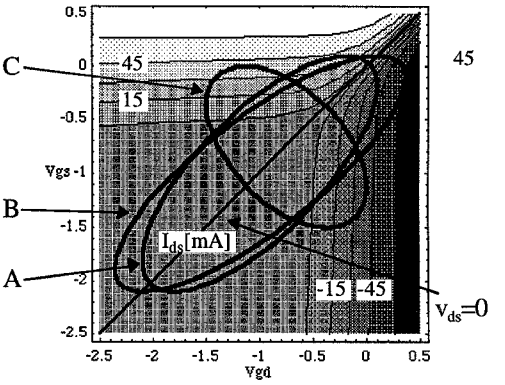

Fig. 4, Contour plot of the channel current versus v_{gs} and v_{gd} for the NE76000 with voltage-trajectories.

Trajectory	$V_{gs,DC}$ [V]	V_{gs}[V]	V_{ds}[V]	φ[deg]
A	-1.00	1.10	0.80	68.6
B	-1.00	1.10	0.80	90.0
C	-0.75	0.75	1.30	29.9

Table 1, Voltages and phase offset for the trajectories

In the above analysis, we have assumed that the voltages in the FET are single tone sinusoidal voltages at the input frequency ω. In practical circuits v_{ds} and v_{gd} will also contain harmonics of ω, especially at the output frequency nω. However these frequency components will be relatively small compared to the one at the input frequency. Therefore, (5) yields a good estimation.

IV. Design

A FET frequency doubler has been designed in microstrip technique in order to verify the above theories. A MESFET from NEC (NE76000) has been used and the substrate(soft) is ARLON iso-clad 933 with ε_r=2.33 and h=0.38 mm. The circuit is kept as simple as possible and the input frequency is low, 1.5 GHz, in order to minimise errors from other effects than the nonlinear behaviour of the FET. A layout of the complete circuit and an equivalent circuit is shown if Fig. 5.

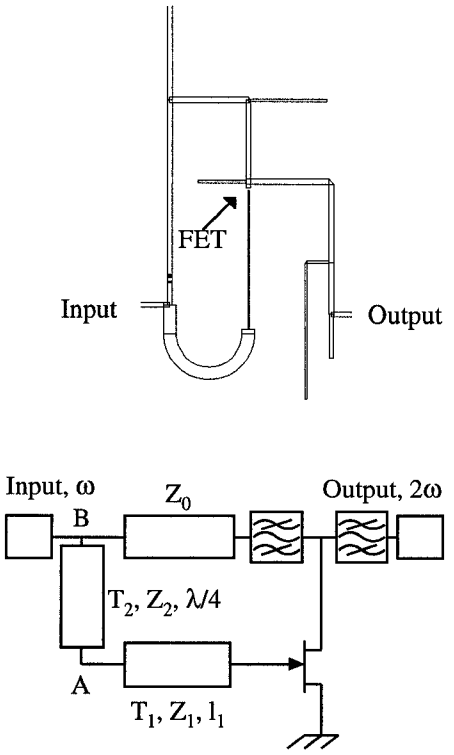

Fig. 5, Layout and equivalent circuit of the doubler.

A general description of the circuit is as follows. The input signal (at the frequency ω) is fed to both the gate and the drain of the FET. It is sufficient to feed only a small part of the input power to the gate. However, the amplitude of v_{gs} should be high to give *g(t)* a rectangular shape. Since the gate is capacitive, high V_{gs} is accomplished by tuning the gate with a piece of high impedance line T_1. The impedance seen towards the gate from point A (Fig. 5) will be a few ohm. To decouple only a small amount of power from point B (Fig. 5), the impedance seen towards the gate from point B (Fig. 5) should be high. This is achieved with a transformer, T_2. The gate voltage can be adjusted to a desired high level by increasing the ratio between the Z_1 and Z_2. The higher ratio between Z_1 and Z_2 the higher Q-value, which decreases the bandwidth. The input and output are matched to 50 ohms by open stubs. The 3ω-harmonic is shorted at the drain with an open stub.

The frequency doubler was optimised for an input power of 3 dBm. The optimum $V_{gs,DC}$ and V_{gs} were found to be -1.2 and 1.7 volts respectively. Fig. 6 shows the simulated voltages and current in the FET. We can see that v_{gs} is a single tone sinusoidal voltage (input frequency) but v_{gd} and v_{ds} are not. When calculating the optimum phase offset, φ, using (5) we get

$$\varphi = Arc\cos(\frac{1.5}{2 \cdot 1.7}) \approx 75° \qquad (8)$$

This agrees well to what we observe in Fig. 6. The voltage v_{gs} and the input frequency voltage component in v_{ds} are linearly dependent on the input power. Therefore the φ will not change with input power.

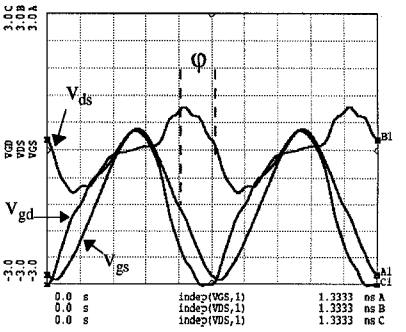

Fig. 6a, Simulated voltages over the FET.

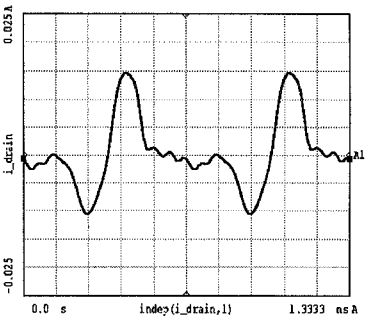

Fig. 6b, Simulated current in the FET-channel.

V. Experimental results

The circuit was mounted in a fixture and the gate-bias voltage was applied externally, with a voltage supply in series with a 2 MΩ resistor. The DC-short at the drain was applied from the outside to enable measurement of the DC-current. The input reflection coefficient was measured with the HP8510C vector network analyser from Hewlett Packard. The measured and simulated input

reflection coefficient for 3 dBm input power is shown in Fig. 7.

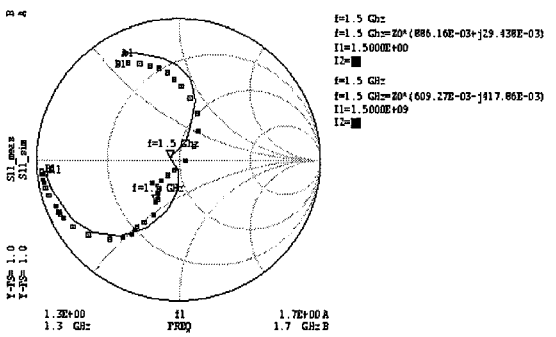

Fig. 7, Simulated and measured input reflection.

Measurements of conversion efficiency and undesired harmonics at the output were made with a the HP8350B signal generator as input source. The output power was measured with the spectrum analyser HP8565E. A correction table for the signal generator and for the surrounding measurement network was established with a power meter, Anritsu ML4803A. In Fig. 8 we can see that an optimum conversion efficiency of -4.5 dB is measured at 1.48 GHz and that the 3dB bandwidth is 10 percent. We also observe that the conversion efficiency is relatively insensitive to the input power. For an input power of -10 to +5 dBm the conversion efficiency is -7.5 to -4.5 dBm. This is shown in Fig. 9. Measurements also showed that the DC-mixing current was below 0.5 mA at center frequency.

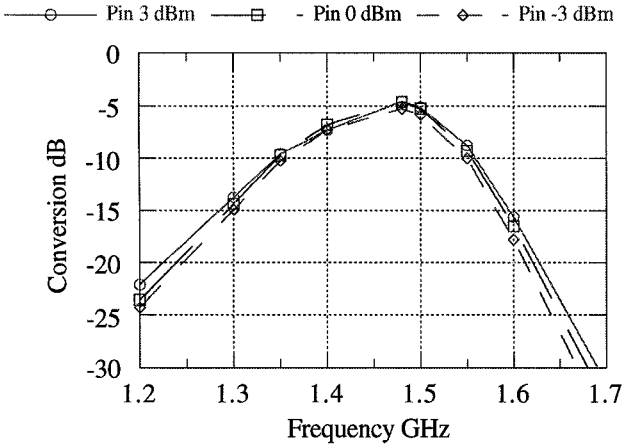

Fig. 8, Measured conversion versus frequency.

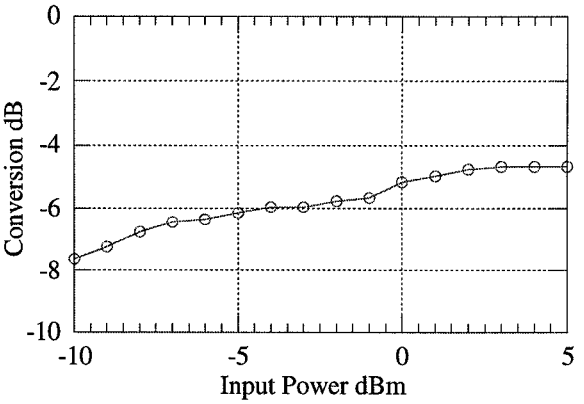

Fig. 9, Measured Conversion vs. P_{in} at 1.48 GHz.

VI. Conclusions

A new type of FET frequency multiplier has been presented. The multiplier works in a similar way as a resistive mixer. It has essentially no DC power dissipation and good stability properties, since the DC voltage over drain-source is zero. Furthermore, the multiplier is insensitive to device parameter variations. Different configurations have been analysed. The first experimental results show a conversion loss of 4.5 dB. We believe that the conversion efficiency can be further improved.

VII. Acknowledgement

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VIII. References

[1] I. Angelov, "A balanced millimeter wave doubler based on pseudomorphic HEMTs", IEEE MTT-S Digest, pp. 353-356, 1992.

[2] T. Hirota, "Uniplanar Monolithic Frequency doublers", IEEE Trans. MTT, vol. 37, no. 8, pp. 1249-1254, Aug. 1989.

[3] A. Gopinath, "Single-Gate MESFET Frequency Doublers", IEEE Trans. MTT, vol. 30, no. 6, pp. 869-875, Jun. 1982.

[4] H. Zirath, "Methods and arrangement for frequency conversion", Patent Pending.

[5] A. Anterov, T. Wilhelmsson, "Frekvensmultiplikatorer baserade på resistivt arbetande FET-transistorer", Diploma Thesis for master of science degree, 1996

[6] A. Saleh, "Theory of resistive mixers", Research monograph #64, M.I.T Press, 1971.